

ASIC ARCHITECHTURE FOR ACTIVE-COMPENSATION
OF A PROGRAMMABLE IMEDANCE I/O

Abstract of the Dislcosure

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A method of, and a circuit for, impedance control. The method comprises the steps of providing an input/output cell having a controllable input/output impedance, providing a reference cell including a node having a variable voltage, and comparing the voltage of the node to a reference voltage. The voltage of the node is adjusted during a defined

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period and according to a defined procedure, and during that defined period, a digital signal is generated. That digital signal is transmitted to the input/output cell to adjust the input/output impedance. Preferably, the circuit is embodied as a digital controller designed as a synthesized core or macro. The advantage of this implementation is that it never has to be redesigned in future technologies. The digital controller may be carried

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over to future technologies in the form of VHDL code, which is pure logic and independent of technology.

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